PATENT ABSTRACTS OF JAPAN

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(54) SAMPLING FREQUENCY CONVERTER

(57)Abstract:
PURPOSE: To prevent accumulation of errors in resampling address time from being generated even when a sampling frequency ratio keeps changing continuously for a prescribed time, to avoid a capacity of a buffer memory from being increased and to eliminate the need for a limit in a changing speed and a changing quantity.
CONSTITUTION: A re-sampling buffer memory 2 stores an input signal Dsi of an input sampling frequency Fsi received from an input terminal 1. An interpolation processing circuit 3 applies interpolation processing to a signal read from the re-sampling buffer memory 2. A sampling frequency ratio detection circuit 7 detects a current sampling frequency ratio Rn of the input sampling frequency Fsi fed from an input terminal 5 to an output sampling frequency Fso fed from an input terminal 6 and detects a new sampling frequency ratio Rn.NEW based on the current sampling frequency ratio Rn and a one-preceding sampling frequency ratio Rn-1. A controller 8 uses the new sampling frequency ratio Rn. NEW to control the re-sampling buffer memory 2 and the interpolation processing circuit 3.

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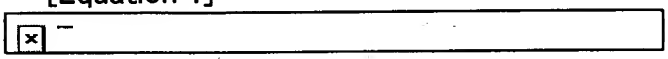
CLAIMS

[Claim(s)]

[Claim 1] In the sampling-frequency inverter which changes the sampling frequency of an input signal into the sampling frequency of arbitration A storage means to memorize the above-mentioned input signal, and the interpolation processing means which carries out interpolation processing of the signal read from the above-mentioned storage means, A sampling-frequency ratio detection means to detect the sampling-frequency ratio of the sampling frequency of the above-mentioned input signal, and the sampling frequency of the above-mentioned arbitration, and to detect a new sampling-frequency ratio based on this detection value and the past detection value, The sampling-frequency inverter characterized by having the control means which controls the above-mentioned storage means and the above-mentioned interpolation processing means according to the new sampling-frequency ratio of the above-mentioned sampling-frequency ratio detection means.

[Claim 2] The above-mentioned sampling-frequency ratio detection means is a sampling-frequency inverter according to claim 1 characterized by subtracting detection value Rn-1 of the past from twice as many value 2Rn as the current detection value Rn, and calculating new sampling frequency-ratio Rn.NEW by the formula of Rn.NEW=2Rn-1.

[Claim 3] a sampling-frequency ratio with the above-mentioned new sampling-frequency ratio detection means -- Rn.NEW -- the difference of the current detection value Rn, this current detection value Rn, and detection value Rn-1 of the past -- the infinite series as a total value of the term from 1 of m of the k (k< 1) double values (1-k) (deltaRn-m) kdeltaRn and m of value deltaRn to infinity -- adding -- [Equation 1]



The sampling-frequency inverter according to claim 1 characterized by asking by the ** type.

[Claim 4] The above-mentioned sampling-frequency ratio detection means is a sampling-frequency inverter according to claim 1 which is a high speed enough, and is the clock of the integral multiple of the sampling frequency of another side, and is characterized by carrying out counting of the period of above-mentioned one sampling frequency to the period of one sampling frequency of the sampling frequency of the above-mentioned input signal, and the sampling frequencies of the above-mentioned arbitration.
[Claim 5] The above-mentioned interpolation processing means is a sampling-frequency inverter according to claim 1 characterized by asking for the exaggerated sampling data of two ********, and giving linear interpolation further to these two exaggerated sampling data by performing over sampling technique processing according to the control signal supplied from the above-mentioned control means to the signal read from the above-mentioned storage means by the above-mentioned control means.
[Claim 6] The sampling-frequency inverter according to claim 1 characterized by band-limiting to the output signal of the above-mentioned interpolation processing means when the sampling frequency of the above-mentioned input signal is higher than the sampling frequency of the above-mentioned arbitration.
[Claim 7] The above-mentioned sampling-frequency ratio detection means detects the sampling-frequency ratio of the sampling time period of the above-mentioned input signal, and the sampling frequency of the above-mentioned arbitration by the short time period and the long time period. this short ********** and this length -- it is -- the current detection value in a time period, and the past detection value -- responding -- the new sampling-frequency ratio in a short time period and a long time period -- detecting -- this -- the sampling-frequency inverter according to claim 1 characterized by switching and outputting two new sampling-frequency ratios.
[Claim 8] coincidence within a predetermined precision of the new sampling-frequency ratio in a time period with the above-mentioned short sampling-frequency ratio detection means, and the new sampling-frequency ratio in a long time period, or an inequality -- distinguishing -- the time of coincidence -- the above -- the sampling-frequency ratio in a long time period -- the time of an inequality -- the above -- the sampling-frequency inverter according to claim 1 characterized by choosing and outputting the sampling-frequency ratio in a short time period.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]

[Industrial Application] This invention relates to the sampling-frequency inverter which re-samples the sampling frequency of an input signal and changes it into the sampling frequency of arbitration.

[0002]

[Description of the Prior Art] Recently, an audio signal is transmitted using an optical cable, a coaxial cable, etc. with a digital signal, and a digital audio signal regenerative apparatus which is reproduced through a digital audio interface came to spread. In this digital audio signal regenerative apparatus, the clock is generated using the phase locked loop (henceforth PLL) which consists of a phase comparator and a voltage controlled oscillator (henceforth VCO) at the time of digital audio signal reception. However, digital one / analog (henceforth D/A) transform-processing property may be degraded for the jitter by VCO of PLL at the time of this clock generation. For this reason, in equipment which reproduces digital audio signal record media, such as a compact disk (henceforth CD) player, and a digital audio tape (henceforth DAT) player, a digital audio signal may be changed into an analog audio signal by D/A transform processing using a quartz watch clock, and it may be said that the good audio signal with more distorted transmitting an analog audio signal after that which is not can be obtained.

[0003] Moreover, in current and the record medium used as the source of a digital audio signal, for example, an optical disk smaller than CD and CD, and the digital audio tape smaller than DAT and DAT, the sampling frequency at the time of digital audio signal record is 44.1kHz, 48kHz, or 32kHz, and is not unified. Moreover, the satellite broadcasting service (henceforth BS) of a sampling frequency which serves as the source of a digital audio signal although it is not a record medium is also either of the above-mentioned sampling frequencies. For this reason, when a sampling frequency, for example, recorded the digital audio signal from DAT and BS whose sampling frequency is 48kHz on the small optical disk which is 44.1kHz, the digital audio signal of DAT and BS this sampling frequency of whose is 48kHz had to be changed into the analog signal by D/A transform processing, it had to change into the digital audio signal whose sampling frequency is 44.1kHz by the analog / digital (henceforth A/D) transform processing again after that, and property degradation by distortion etc. was not avoided.

[0004] Moreover, it is necessary to mix, after changing respectively into an analog signal each digital audio signal set as the object of mixing when carrying out mixing sound recording of the digital audio signal using DAT, when a sampling frequency differs from the synchronous approach.

[0005] As mentioned above, in order to prevent the performance degradation by generating of a clock jitter, and degradation of the playback digital audio signal by different sampling frequency and to realize digital mixing by free sampling-frequency conversion, development of an asynchronous sampling-frequency inverter has been desired.

[0006] Generally, this sampling-frequency inverter uses the re-sampling time amount address for specification of the point for re-sampling the signal inputted with the sampling frequency Fsi with a sampling frequency Fso sampling [re-]. This re-sampling time amount address is generated according to the ratio of the sampling frequency (henceforth an input sampling frequency) Fsi of an input signal, and the sampling frequency (henceforth an output sampling frequency) Fso of the signal re-sampled.

[0007] Specifically the sampling-frequency ratio R of the input sampling frequency Fsi and the output sampling frequency Fso The period of the output sampling frequency Fso (it is hereafter called an output sampling period.) It is a M times as many input-reference clock (it is hereafter called an input master clock.) as the input sampling frequency Fsi in one (= N, Tso) N times the period t of Tso. By carrying out counting by MCKi (=M-Fsi), it detected equalizing and removing jitter components, such as Fsi, MCKi, and Fso, accumulation of this sampling-frequency ratio R and the re-sampling time amount was carried out, and the re-sampling time amount address was generated. And the sampling frequency was changed by reading the point stored in the buffer memory for re-sampling sampling [re-] with this re-sampling time amount address.

[0008]

[Problem(s) to be Solved by the Invention] By the way, in order to perform conversion for obtaining a re-sampling frequency using highly precise sampling-frequency conversion, i.e., the re-sampling time amount address, it is necessary to improve the resolution of the re-sampling time amount address. For this reason, it is possible to increase the detection period (time amount) t which enlarges the above-mentioned scale factor N and detects the sampling-frequency ratio R of the input sampling frequency Fsi and the output sampling frequency Fso. However, un-arranging [that an error will arise in the value of the sampling-frequency ratio R and actual Fsi/Fso in excessive in an application which carries out adjustable / of the input sampling frequency Fsi and the output sampling frequency Fso / in this case] will arise.

[0009] For this reason, conversion of a highly precise sampling frequency was realized under the conditions that a sampling frequency Fsi and the re-sampling frequency Fso are fixed.

[0010] Moreover, when a sampling-frequency ratio continues changing continuously during 1 scheduled time, there is a possibility of the error of the re-sampling time amount address being accumulated, and exceeding the capacity of buffer memory, and a limit of a change rate and variation and increase of buffer memory were caused. In an application which carries out adjustable [of the input sampling frequency Fsi and the output sampling frequency Fso] as mentioned above, this is because error deltaR will arise, as shown in the value of the sampling-frequency ratio R, and actual Fsi/Fso at drawing 13 .

[0011] Making high the above-mentioned input master clock MCKi, and, improving the

resolution of the re-sampling time amount address regardless of compaction of the above-mentioned detection period t on the other hand, is also considered. However, the limitation of circuit working speeds, such as a counter, and the problem of absorption removal of an input-clock jitter arise in this case. For this reason, although reduction in with error was enabled even if it is going to make high simply the frequency of the above-mentioned input master clock MCKi and was going to raise the resolution of the re-sampling time amount address, prevention of accumulation with error was not enabled.

[0012] This invention aims at offer of the sampling-frequency inverter which makes a limit of a change rate and variation unnecessary, without not generating accumulation of the error of the re-sampling time amount address, and therefore increasing the capacity of buffer memory, even if it is made in view of the above-mentioned actual condition and a sampling-frequency ratio continues changing continuously during 1 scheduled time.

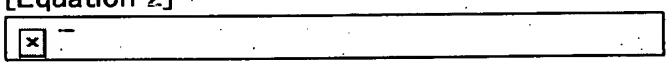
[0013]

[Means for Solving the Problem] In the sampling-frequency inverter from which the sampling-frequency inverter concerning this invention changes the sampling frequency of an input signal into the sampling frequency of arbitration A storage means to memorize the above-mentioned input signal, and the interpolation processing means which carries out interpolation processing of the signal read from the above-mentioned storage means, A sampling-frequency ratio detection means to detect the sampling-frequency ratio of the sampling frequency of the above-mentioned input signal, and the sampling frequency of the above-mentioned arbitration, and to detect a new sampling-frequency ratio based on this detection value and the past detection value, The above-mentioned technical problem is solved by having the control means which controls the above-mentioned storage means and the above-mentioned interpolation processing means according to the new sampling-frequency ratio of the above-mentioned sampling-frequency ratio detection means.

[0014] In this case, the above-mentioned sampling-frequency ratio detection means subtracts detection value Rn-1 of the past from twice as many value 2Rn as the current detection value Rn, and you may make it calculate new sampling frequency-ratio Rn.NEW by the formula of Rn.NEW=2Rn-1.

[0015] moreover, a sampling-frequency ratio with the above-mentioned new sampling-frequency ratio detection means -- Rn.NEW -- the difference of the current detection value Rn, this current detection value Rn, and detection value Rn-1 of the past -- the infinite series as a total value of the term from 1 of m of the k (k< 1) double values (1-k) (deltaRn-m) kdeltaRn and m of value deltaRn to infinity -- adding -- [0016]

[Equation 2]



[0017] You may make it ask by the ** type.
[0018] Moreover, the above-mentioned sampling-frequency ratio detection means is a high speed enough, and is the clock of the integral multiple of the sampling frequency of another side, and you may make it detect a sampling-frequency ratio to the period of one sampling frequency of the sampling frequency of the above-mentioned input signal, and the sampling frequencies of the above-mentioned arbitration by carrying out counting of the period of above-mentioned one sampling frequency.
[0019] Moreover, as for the above-mentioned interpolation processing means, it is desirable to ask for the exaggerated sampling data of two ********, and to perform linear interpolation processing to these two exaggerated sampling data further by performing over sampling technique processing according to the control signal supplied from the above-mentioned control means to the signal read from the above-mentioned storage means by the above-mentioned control means.
[0020] Here, two exaggerated sampling data based on the above-mentioned over sampling technique processing are obtained with two non-recursive filters.
[0021] Moreover, when the sampling frequency of the above-mentioned input signal is higher than the sampling frequency of the above-mentioned arbitration, it is desirable to band-limit to the output signal of the above-mentioned interpolation processing means.
[0022] moreover, a time period with the above-mentioned short sampling-frequency ratio detection means and a long time period -- the sampling-frequency ratio of the sampling time period of the above-mentioned input signal, and the sampling frequency of the above-mentioned arbitration -- detecting -- this short ********** and this merit -- it is -- the current detection value in a time period, and the past detection value -- responding -- the new sampling-frequency ratio in a short time period and a long time period -- detecting -- this -- it is desirable to switch and output two new sampling-frequency ratios.
[0023] moreover, coincidence within a predetermined precision of the new sampling-frequency ratio in a time period with the above-mentioned short sampling-frequency ratio detection means, and the new sampling-frequency ratio in a long time period or an inequality -- distinguishing -- the time of coincidence -- the above -- the sampling-frequency ratio in a long time period -- the time of an inequality -- the above -- the sampling-frequency ratio in a short time period is chosen, and you may make it output
[0024] Distinction of this coincidence or an inequality is performed by comparing the sampling-frequency ratio in a short time period with the sampling-frequency ratio in a long time period with a comparison means. It can carry out, when only the range of a predetermined digit count compares the sampling-frequency ratio in a long time period, and the sampling-frequency ratio in a short time period with distinction within a predetermined precision. For example, when treating a sampling-frequency ratio as digital value, it is because a predetermined bit [most significant bit / of a sampling-

frequency ratio with much number of bits] (for example, it responded to the total number of bits of a sampling-frequency ratio with little number of bits) and all the bits of a sampling-frequency ratio with little number of bits are measured.
[0025] Moreover, the above-mentioned control means supplies the above-mentioned re-sampling time amount address and the data write-in address which are the data read-out address to the above-mentioned storage means. Moreover, the above-mentioned control means supplies the selection-control signal of the over sampling technique multiplier used for the above-mentioned over sampling technique processing by the above-mentioned interpolation processing means, and the linear interpolation multiplier for the object for precedence leading, and following trailing used for the above-mentioned linear interpolation processing.
[0026]
[Function] A sampling-frequency ratio detection means detects the sampling-frequency ratio of the sampling frequency of an input signal, and the sampling frequency of arbitration, and outputs it to a control means in quest of a new sampling-frequency ratio based on this current detection value and the detection value of the past in front of 1 detection period. For this reason, a limit of a change rate and variation is made unnecessary, without not generating accumulation of the error of the re-sampling time-of-day address, and therefore increasing the capacity of buffer memory, even if a sampling-frequency ratio continues changing continuously during 1 scheduled time since a control means controls a storage means and a interpolation processing means according to a new sampling-frequency ratio.
[0027]
[Example] Hereafter, the desirable example of the sampling-frequency inverter concerning this invention is explained, referring to a drawing.
[0028] First, the 1st example is explained, referring to drawing 1 . This 1st example is a sampling-frequency inverter which re-samples the sampling frequency Fsi of the signal Dsi inputted from the input terminal 1, and changes it into the signal Dso of the sampling frequency Fso of arbitration, and an I/O system realizes completely asynchronous sampling-frequency transform processing, i.e., sampling-frequency transform processing of a free ratio without synchronous relation between I/O signals. Hereafter, make the sampling frequency Fsi of an input signal Dsi into the input sampling frequency Fsi, and let the sampling frequency Fso of arbitration be the output sampling frequency Fso.
[0029] The buffer memory 2 for re-sampling read while the sampling-frequency inverter of this 1st example writes in the input signal Dsi of the input sampling frequency Fsi inputted from the input terminal 1, The interpolation processing circuit 3 which interpolates the output signal of this buffer memory 2 for re-sampling, The sampling-frequency ratio Rn is detected from the above-mentioned input sampling-frequency Fsi information supplied from an input terminal 5, and the above-mentioned output sampling-frequency Fso information supplied from an input terminal 6. This

current detection value Rn and the sampling-frequency ratio detector 7 which detects new sampling frequency-ratio Rn.NEW based on detection value Rn-1 of the past in front of 1 detection period, It has from Rn.NEW the controller 8 which controls the buffer memory 2 for re-sampling, and the interpolation processing circuit 3. the new sampling-frequency ratio of this sampling-frequency ratio detector 7 -- The interpolation processing circuit 3 where interpolation processing was performed by this controller 8 outputs the signal Dso of the output sampling frequency Fso from an output terminal 4.

[0030] The sampling-frequency ratio detector 7 subtracts detection value Rn-1 of the past from one twice the value of the current sampling-frequency ratio Rn, and calculates new sampling frequency-ratio Rn.NEW. This is because it is referred to as new sampling frequency-ratio Rn.NEW by adding subtraction value deltaRn of the present sampling-frequency ratio Rn and detection value Rn-1 of the past to the present sampling-frequency ratio Rn, as shown in drawing 5 . Namely, new sampling frequency-ratio Rn.NEW Rn. NEW=Rn+delta Rn=Rn+(Rn-Rn -1) =2 Rn-Rn -1 ... (1)
It becomes. This new sampling frequency-ratio Rn.NEW is outputted to a controller 8.

[0031] the new sampling-frequency ratio to which a controller 8 is supplied from the sampling-frequency ratio detector 7 -- according to Rn.NEW, the re-sampling time amount address which is the data read-out address is generated, and the buffer memory 2 for re-sampling is supplied. Moreover, the controller 8 also supplies the data write-in address to the buffer memory 8 for re-sampling. moreover, the controller 8 -- the above -- a new sampling-frequency ratio -- according to Rn.NEW, the selection-control signal of the over sampling technique multiplier used for the over sampling technique processing performed in the interpolation processing circuit 3 and the linear interpolation multiplier for the object for precedence leading and following trailing used for linear interpolation processing are generated, and this interpolation processing circuit 3 is supplied.

[0032] The interpolation processing circuit 3 reads a required data constellation from the buffer memory 2 for re-sampling based on the above-mentioned re-sampling time amount address, for example, makes the high order interpolation data of two ******** corresponding to the re-sampling time amount address by form [where it does not go round] (henceforth FIR) filtering, and generates the signal Dso of the output sampling frequency Fso further by adding, after giving linear interpolation of the data in each.

[0033] Therefore, the sampling-frequency inverter of this 1st example measures the current sampling-frequency ratio Rn from the input sampling frequency Fsi and the output sampling frequency Fso, calculates new sampling frequency-ratio Rn.NEW based on detection value Rn-1 of this current detection value Rn and the past, and is outputting it to the controller 8. For this reason, a controller 8 can perform stable sampling transform processing, without not making the buffer memory 2 for re-sampling produce overflow and an underflow, but increasing the capacity of the buffer

memory 2 for re-sampling, since the re-sampling time amount address is generable from the value (new sampling-frequency ratio Rn. NEW) which an error like drawing 5 does not accumulate.

[0034] Next, it explains, referring to drawing 3 thru/or drawing 5 about the 2nd example. As this 2nd example is also shown in drawing 3 , it is the sampling-frequency inverter which re-samples the sampling frequency Fsi of the signal Dsi inputted from the input terminal 11, and changes it into the signal Dso of the sampling frequency Fso of arbitration like the 1st example mentioned above, and an I/O system realizes completely asynchronous sampling-frequency transform processing, i.e., sampling-frequency transform processing of a free ratio without synchronous relation between I/O signals. Hereafter, make the sampling frequency Fsi of an input signal Dsi into the input sampling frequency Fsi, and let the sampling frequency Fso of arbitration be the output sampling frequency Fso.

[0035] 8Fs over sampling technique filter 12 which carries out over sampling technique processing of the input signal Dsi of the input sampling frequency Fsi inputted from the input terminal 11 at 8Fsi(s) for re-sampling as the sampling-frequency inverter of this 2nd example is shown in drawing 3 , The buffer memory 13 for re-sampling read while writing in the input signal set to 8Fs(es) with this 8Fs over sampling technique filter 12, The input-reference clock of the integral multiple of the interpolation processing circuit 14 which interpolates the output signal of this buffer memory 13 for re-sampling, and the sampling frequency Fsi supplied from an input terminal 22 (it is hereafter called an input master clock.) The period of the sampling frequency Fso supplied from an input terminal 23 by MCKi (=M-Fsi) (it is hereafter called an output sampling period.) The current sampling-frequency ratio Rn which improved resolution by carrying out counting of one (= N, Tso) N times the period t of Tso is measured. this current sampling-frequency ratio Rn and the sampling-frequency ratio of the past in front of 1 detection period -- Rn-1 -- being based -- a new sampling-frequency ratio -- the sampling-frequency ratio detector 24 which calculates Rn.NEW -- the new sampling-frequency ratio detected in this sampling-frequency ratio detector 24 -- by the controller 25 which controls the buffer memory 13 for re-sampling, and the interpolation processing circuit 14 according to Rn.NEW, and this controller 25 While operating on a curtailed schedule the sampling frequency of the output signal from the interpolation processing circuit 14 by which interpolation processing was controlled, for example, carrying out to one 4 or 8 times the output sampling frequency [2 and] Fso of this And the re-sampling-frequency signal output circuit 19 which switches the 1 by multiplexer 19a, and chooses it, It band-limits to an output signal from this re-sampling-frequency signal output circuit 19, and it has the band limit filter 20 which outputs the output signal Dso of the output sampling frequency Fso, and consists of an output termina! 21.

[0036] Although the digital signal of sampling-frequency 8Fsi made from 8Fs over sampling technique SHIRUTA 12 is inputted into the buffer memory 13 for re-

sampling as mentioned above, this buffer memory 13 for re-sampling is the 20-bit 64-word buffer RAM, and serves as a 8 times as many buffer as input sampling-frequency time amount.

[0037] The sampling-frequency ratio detector 24 comes to have the counter 30 which carries out counting of sampling-period Ns-Tso of the integral multiple in the time period t inputted from input terminal 23a by the input master clock MCKi supplied from an input terminal 22, and the latch 31 who latches the count output from this counter 30 based on above-mentioned Ns-Tso, as that configuration is shown in drawing 4 .

[0038] The current sampling-frequency ratio Rn in a period ts will be called for by counting Ns-Tso with the input master clock MCKi with a counter 30, and latching the count result by latch 31.

[0039] Like the sampling-frequency ratio detector 7 of the 1st example mentioned above, this sampling-frequency ratio detector 4 subtracts detection value Rn-1 of the past in front of 1 detection period from one twice the value of the current sampling-frequency ratio Rn, and calculates new sampling frequency-ratio Rn.NEW. This is because it is referred to as new sampling frequency-ratio Rn.NEW by adding subtraction value deltaRn of the present sampling-frequency ratio Rn and detection value Rn-1 of the past to the present sampling-frequency ratio Rn, as shown in drawing 2 . That is, new sampling frequency-ratio Rn.NEW is similarly indicated to be the above-mentioned (1) formula.

[0040] As the configuration is shown in drawing 4 , a controller 25 carries out accumulation of the new sampling frequency-ratio Rn.NEW supplied from the sampling-frequency ratio detector 24 using an adder circuit 32 and a flip-flop circuit 32, and is generating the data read-out address of the buffer memory 13 for re-sampling. moreover, the controller 25 -- an adder circuit 32 and a flip-flop circuit 33 -- using -- the multiplier for the over sampling techniques to the interpolation processing circuit 14 -- a selection system -- linear interpolation multiplier LIP.F.L for the signal to print, and the objects for precedence leading and following trailing and LIP.F.T are generated.

[0041] These data read-out address, the multiplier selection-control signal for over sampling techniques, and a linear interpolation multiplier are outputted from this controller 25 as data of the high-order-bit range of one data stream, the middle bit range, and the lower bit range.

[0042] Here, as for a flip-flop circuit 33, it is desirable that it is a D-flip-flop circuit, and the clock of 8 in all Fso(es) is supplied to sampling-frequency 8Fso of the output signal of this 2nd example from the input terminal 34. Of course, when the sampling frequency of an output signal is 4 or 2Fso(es), the clock of 4 or 2Fso(es) is supplied. Moreover, an initialization signal is supplied from an input terminal 35.

[0043] As the interpolation processing circuit 14 is shown in drawing 3 , while performing over sampling technique processing to the data read from the buffer

memory 13 for re-sampling by the re-sampling time amount address which is the data read-out address supplied from the above-mentioned controller 25 FIR (filter L) &xLIP.F.L15 and FIR (filter T) &xLIP.F.T17 which give linear interpolation, The multiplier ROM 16 which supplies the multiplier for over sampling techniques to these FIR (filter L) &xLIP.F.L15 and FIR (filter T) &xLIP.F.T17 It has the adder 18 adding the output signal of FIR (filter L) &xLIP.F.L15, and the output signal of FIR (filter T) &xLIP.F.T17, and changes. Here, the multiplier ROM 16 has 32 24-bit over sampling technique multipliers of 7 words.

[0044] Actuation of this interpolation processing circuit 14 is explained referring to drawing 5 . The buffer memory 13 for re-sampling supplies Tsi / seven data for every eight as shown in FIR (filter L) &xLIP.F.L15 and FIR (filter T) &xLIP.F.T17 at (A) of drawing 5 based on the read-out address supplied from a controller 25. FIR (filter L) &xLIP.F.L15 and FIR (filter T) &xLIP.F.T17 carry out the sum-of-products operation of the multiplier of seven pieces which was supplied from the buffer memory 13 for re-sampling and which was read from the multiplier ROM 16, for example to seven data, and generate the data of 256Fsi(s), respectively.

[0045] (B) of drawing 5 shows the data of two ******** of this data of 256Fsi(s). The broken-line envelopment field E1 shown in (A) of drawing 5 and (B) of drawing 5 is Tsi/8, and the broken-line envelopment field E2 shown in (B) of drawing 5 is data of two ******** of 256Fsi(s) of Tsi/256 spacing.

[0046] Next, after FIR (filter L) &xLIP.F.L15 and FIR (filter T) &xLIP.F.T17 multiply the data of two ******** of Tsi/256 spacing by the linear interpolation multiplier supplied from a controller 25, they are added with an adder 18, and they perform linear interpolation as shown in (C) of drawing 5 .

[0047] By repeating such over sampling technique and linear interpolation, this 2nd example generates the data Dso of the sampling frequency Fso as shown in (D) of drawing 5 .

[0048] Here, the linear interpolation multiplier is explained. As a linear interpolation multiplier, there are multiplier LIP.F.L for leading lead data and multiplier LIP.F.T for trailing following data. These linear interpolation multipliers are generated in a controller 25 using the data of the low order of the value by which accumulation was carried out, for example, 12 bits. Specifically, low order 12 bit data and multiplier LIP.F.L for leading lead data are given for multiplier LIP.F.T for trailing following data by the one's complement of 12 bits of low order.

[0049] The data Dso which carried out the multiplication of the above-mentioned linear interpolation multiplier, and obtained it are shown in two data Dsa and Dsb of Tsi/256 spacing in the broken-line envelopment field E3 at (C) of drawing 5 .

[0050] The data outputted from the interpolation processing circuit 14 are data of 8Fso(es). This data of 8Fso(es) is supplied to the re-sampling-frequency signal output circuit 19. This re-sampling-frequency signal output circuit 19 performed infanticide processing to 8Fso, changed it into 4Fso or 2Fso(es), and has switched and chosen

one of 8Fso, 4Fso, or the 2Fso(es) by multiplexer 19a.
[0051] The band limit filter 20 is a filter for not making output data generate an aliasing noise. Since there is a possibility that an aliasing noise may occur when the 1st sampling frequency FSi is higher than the output sampling frequency Fso, the output signal from multiplexer 19a is band-limited.
[0052] Therefore, the sampling-frequency inverter of this 2nd example measures the current sampling-frequency ratio Rn from the input sampling frequency Fsi and the output sampling frequency Fso, calculates new sampling frequency-ratio Rn.NEW based on detection value Rn-1 of this current detection value Rn and the past, and is outputting it to the controller 25. For this reason, a controller 25 can perform stable sampling transform processing, without not making the buffer memory 13 for re-sampling produce overflow and an underflow, but increasing the capacity of the buffer memory 13 for re-sampling, since the re-sampling time amount address is generable from the value (new sampling-frequency ratio Rn. NEW) which an error like drawing 2 does not accumulate. Furthermore, the output signal Dso of the sampling frequency Fso used as an output signal turns into a signal without aliasing.
[0053] Next, it explains, referring to drawing 6 thru/or drawing 8 about the 3rd example. It is the sampling-frequency inverter which re-samples the sampling frequency Fsi of the inputted signal Dsi, and changes it into the signal Dso of the sampling frequency Fso of arbitration like [this 3rd example] the 1st example and the 2nd example which were mentioned above, and an I/O system realizes completely asynchronous sampling-frequency transform processing, i.e., sampling-frequency transform processing of a free ratio without synchronous relation between I/O signals. Hereafter, make the sampling frequency Fsi of an input signal Dsi into the input sampling frequency Fsi, and let the sampling frequency Fso of arbitration be the output sampling frequency Fso. Moreover, drawing 3 which showed the outline configuration of the 2nd example can show the outline configuration of this 3rd example. The difference of this 3rd example and 2nd example is actuation at the concrete configuration list of the sampling-frequency ratio detector 24.
[0054] Hereafter, although this 3rd example is explained newly referring to drawing 6 thru/or drawing 8 with drawing 3 , since it mentioned above, explanation is advanced to the concrete configuration list of the sampling-frequency ratio detector 24 focusing on actuation.
[0055] As the sampling-frequency inverter of this 3rd example is shown in drawing 3 , 8Fs over sampling technique filter 12, The period of the sampling frequency Fso supplied from an input terminal 23 with the input master clock MCKi of the integral multiple of the buffer memory 13 for re-sampling, the interpolation processing circuit 14, and the sampling frequency Fsi supplied from an input terminal 22 (= M-Fsi) (it is hereafter called an output sampling period.) The sampling-frequency ratio which improved resolution by carrying out counting of one (=N-Tso) N times the period t of Tso by the short time period ts and the long time period tL by the short time period

ts and the long time period tL It detects, respectively. The current detection values Rns and RnL in the short time period ts and the long time period tL, Based on detection value Rns-1 of the past, and RnL-1, new sampling frequency-ratio Rns.NEW in the short time period ts and the long time period tL and RnL.NEW are detected. this -- a new sampling-frequency ratio -- with the sampling-frequency ratio detector 24 which switches and outputs Rns.NEW and RnL.NEW It is a control signal generation means to generate the control signal which controls the buffer memory 13 for re-sampling, and the interpolation processing circuit 14 from Rns.NEW and RnL.NEW. the new sampling-frequency ratio detected in this sampling-frequency ratio detector 24 -- And it has the controller 25 and the re-sampling-frequency signal output circuit 19 which are a control means, and the band limit filter 20, and changes.

[0056] As the configuration is shown in drawing 6 , the sampling-frequency ratio detector 24 with the input master clock MCKi supplied from an input terminal 22 The short period counter 40 which carries out counting of sampling-period Ns-Tso of the integral multiple in the short time period ts inputted from input terminal 23a, With the latch 41 who latches the count output from this short period counter 40 based on above-mentioned Ns-Tso The long period counter 42 which carries out counting of sampling-period NL-Tso of the integral multiple in the long time period tL inputted from input terminal 23b by the input master clock MCKi supplied from an input terminal 22, With the latch 43 who latches the count output from this long period counter 42 based on Above NL and Tso It comes to have the comparator circuit 44 which measures latch's 41 latch output, and latch's 43 latch output, and the selection circuitry 45 which has responded to the comparison result in this comparator circuit 44, shifts, and chooses and outputs that latch output to a controller 25.

[0057] The current sampling-frequency ratio Rns in the short period ts will be called for by counting Ns-Tso with the input master clock MCKi by the short period counter 40, and latching the count result by latch 41. Moreover, the current sampling-frequency ratio RnL in the long period tL will be called for by counting NL-Tso with the input master clock MCKi by the long period counter 42, and latching the count result by latch 43. That is, the latch period in latch 41 is the short period ts, and the latch period in latch 43 is the long period tL. It is determined that the resolution of these latch periods ts and tL of the error and the sampling-frequency ratio Rns to the real time of the sampling-frequency ratio RnL in the conversion at the time of the I/O sampling-frequency ratio rate-of-change max assumed will correspond.

[0058] Here, the input master clock MCKi is high-speed enough to Ns-Tso and NL-Tso, and as mentioned above, it is the clock of the integral multiple M of the input sampling frequency Fsi.

[0059] this sampling-frequency ratio detector 4 -- the sampling-frequency ratio of the past in front of 1 detection period in the current short period ts from the sampling-frequency ratio Rns and the current sampling-frequency ratio RnL in the long period tL and the current long period tL in the short period ts -- Rns-1 and

RnL-1 -- asking -- the new-sampling-frequency ratio in the still shorter time period ts from each of these detection values, and the long time period tL -- Rns.NEW and RnL.NEW are detected.

[0060] In the short period ts, the sampling-frequency ratio detector 24 subtracts detection value Rns-1 of the past from the current ratio Rns twice the value of a sampling frequency, and detects new sampling frequency-ratio Rns.NEW. This is because it is referred to as new sampling frequency-ratio Rns.NEW by adding subtraction value deltaRns of the present sampling-frequency ratio Rns and detection value Rns-1 of the past to the present sampling-frequency ratio Rns, as shown in drawing 7 . Namely, new sampling frequency-ratio Rns.NEW Rns. NEW=Rns+delta Rns=Rns+(Rns-Rns -1) =2 Rns-Rns -1 ... (2)
It becomes.

[0061] In the long period tL, the sampling-frequency ratio detector 24 subtracts detection value RnL-1 of the past from the current ratio RnL twice the value of a sampling frequency, and detects new sampling frequency-ratio RnL.NEW. This is because it is referred to as new sampling frequency-ratio RnL.NEW by adding subtraction value deltaRnL of the present sampling-frequency ratio RnL and detection value RnL-1 of the past to the present sampling-frequency ratio RnL, as shown in drawing 8 . Namely, new sampling frequency-ratio RnL.NEW RnL. NEW=RnL+delta RnL=RnL+(RnL-RnL -1) =2 RnL-RnL -1 ... (3)
It becomes.

[0062] a sampling-frequency ratio with a new comparator circuit 44 -- Rns.NEW and a new sampling-frequency ratio -- RnL.NEW is in agreement within a predetermined precision, or it distinguishes whether it is inharmonious. If new sampling frequency-ratio Rns.NEW and new sampling frequency-ratio RnL.NEW distinguish from coincidence or an inequality in this comparator circuit 44, this comparator circuit 44 will supply the selection-control signal according to that information to a selection circuitry 45.

[0063] A selection circuitry 45 switches, chooses and outputs new sampling frequency-ratio Rns.NEW or new sampling frequency-ratio RnL.NEW from latch 41 or latch 43 according to the selection-control signal supplied from the comparator circuit 44.

[0064] the new sampling-frequency ratio which is a value with many comparison in a comparator circuit 44 to the number of bits -- the new sampling-frequency ratio which are RnL.NEW and a value with little number of bits -- although Rns.NEW is compared -- the time of the comparison -- for example, a sampling-frequency ratio -- up to a predetermined bit (a sampling-frequency ratio -- it responded to the total number of bits of Rns.NEW) from the most significant bit of RnL.NEW -- a sampling-frequency ratio -- it is because all the bits of Rns.NEW are measured. If it does in this way, the coincidence and inequality can be distinguished within the limits of predetermined. a sampling-frequency ratio with this new comparator circuit 44 --

RnL.NEW and a new sampling-frequency ratio -- if Rns.NEW is in agreement within a predetermined precision and it will distinguish -- a selection circuitry 45 -- the new sampling-frequency ratio in the long period ts -- the selection-control signal "choose and output RnL.NEW" is supplied. a sampling-frequency ratio with this comparator circuit 44 new on the other hand -- RnL.NEW and a new sampling-frequency ratio -- Rns.NEW is inharmonious within a predetermined precision -- if it distinguishes -- a selection circuitry 45 -- the new sampling-frequency ratio in the short period tL -- the selection-control signal "choose and output Rns.NEW" is supplied.

[0065] A selection circuitry 45 outputs new sampling frequency-ratio Rns.NEW in new sampling frequency-ratio RnL.NEW or the new short period ts in the long period tL to the adder 46 of a controller 25 with the two above-mentioned selection-control signals supplied from a comparator circuit 44.

[0066] the new sampling-frequency ratio in the long period tL supplied from the sampling-frequency ratio measurement circuit 24 as a controller 25 shows the configuration to drawing 6 -- the new sampling-frequency ratio in RnL.NEW or the short period ts -- accumulation of the Rns.NEW is carried out using an adder circuit 46 and a flip-flop circuit 47, and the data read-out address of the buffer memory 13 for re-sampling is generated. Moreover, the controller 25 is generating the multiplier read-out address for the over sampling techniques to the interpolation processing circuit 14, and the linear interpolation multiplier for linear interpolation using an adder circuit 46 and a flip-flop circuit 47.

[0067] Here, as for a flip-flop circuit 47, it is desirable that it is a D-flip-flop circuit, and the clock of 8 in all Fso(es) is supplied to sampling-frequency 8Fso of the output signal of this 3rd example from the input terminal 48. Of course, when the sampling frequency of an output signal is 4 or 2Fso(es), the clock of 4 or 2Fso(es) is supplied. Moreover, an initialization signal is supplied from an input terminal 49.

[0068] Since the outline configuration and actuation of the interpolation processing circuit 14 are the same as that of it of the 2nd above-mentioned example which was explained while referring to drawing 3 and drawing 5 , explanation is omitted here.

[0069] Therefore, the sampling-frequency inverter of this 3rd example With the input master clock MCKi of the integral multiple of the input sampling frequency Fsi (=M-Fsi), a period (= N, Tso) N times the period t of a sampling frequency Fso The sampling-frequency ratio which improved resolution by carrying out counting by the short time period ts and the long time period tL by the short time period ts and the long time period tL It detects, respectively. The current detection values Rns and RnL in the short time period ts and the long time period tL, Based on detection value Rns-1 of the past, and RnL-1, new sampling frequency-ratio Rns.NEW in the short time period ts and the long time period tL and RnL.NEW are detected. the new sampling-frequency ratio in this short period ts -- the new sampling-frequency ratio in Rns.NEW and the long period tL, when RnL.NEW is in agreement within a predetermined precision New sampling frequency-ratio RnL.NEW in the long period tL

in the case of an inequality Accumulation of the new sampling frequency-ratio RnL.NEW in the short period ts is carried out. Since control signals, such as the sampling data read-out address, a ROM multiplier selection-control signal, and a linear interpolation multiplier, are created and the buffer memory 13 for re-sampling and the interpolation processing circuit 14 are controlled by this control signal Stable sampling transform processing can be performed without not making the buffer memory 13 for re-sampling produce overflow and an underflow, but increasing the capacity of the buffer memory 13 for re-sampling. Moreover, the output signal Dso of the sampling frequency Fso used as an output signal is not made to cause aliasing. furthermore, degradation prevention of the playback audio data signal by sampling-frequency ratio which switches accommodative whether the response of the control signal of the re-sampling data read-out address etc. is made into a high speed according to a sampling-frequency ratio or it is supposed that it is highly precise, and is different in it, and implementation of mixing by free sampling-frequency conversion can be aimed at.

[0070] In addition, three or more re-sampling-frequency ratio measurement circuits are prepared, and the re-sampling-frequency inverter concerning this invention can also be finely dealt with high degree of accuracy and a high-speed response.

[0071] Moreover, the re-sampling-frequency inverter concerning this invention can also consider a sampling-frequency ratio detector as a configuration like drawing 9 . The example which prepared the sampling-frequency ratio detector as shown in this drawing 9 is explained below as other examples. In addition, since other examples are considered as the configuration which changed only the sampling-frequency ratio detector with the sampling-frequency inverter of the 3rd example of the above, the explanation about other configurations is omitted here.

[0072] A short period counter and a long period counter are not prepared independently like [when other examples constitute a sampling-frequency ratio detector] the 3rd example mentioned above. To the sampling-frequency ratio Rs of the short period sampling-frequency ratio detector 53 equipped with the short period counter, share the adder circuit 44 for the re-sampling time-of-day address generation of a controller by time sharing, and accumulation is given. He is trying to obtain new sampling frequency-ratio Rn.NEW accommodative, and a long period counter can be omitted.

[0073] Namely, the sampling-frequency ratio detector of other examples New sampling frequency-ratio Rns.NEW in the short period ts which carried out counting of the sampling frequency Fsi of the signal inputted from an input terminal 52, and asked for it with the dividing clock supplied from the clock counting-down circuit 51, this sampling-frequency ratio -- by carrying out accumulation of the Rns.NEW using an adder circuit 54 and the accumulation latch 55, and carrying out counting using a dividing clock by the long period latch 56 The coincidence with new sampling frequency-ratio RnL.NEW or the inequality in the obtained long period tL is detected

within a precision predetermined in a comparator circuit 57. At the time of coincidence, a selection circuitry 58 chooses sampling frequency-ratio RnL.NEW in the long period tL, chooses sampling frequency-ratio Rns.NEW in the short period ts at the time of an inequality, and it outputs to a controller. Here, the clock counting-down circuit 51 carries out dividing of the reference clock supplied from an input terminal 50, and supplies the dividing clock to the short period sampling-frequency ratio detector 53, the accumulation latch circuit 55, and the long period latch circuit 56.

[0074] therefore, other examples change a highly precise sampling frequency, when it switches accommodative whether the response of generation of the re-sampling time amount address is made highly precise according to a sampling-frequency ratio, using the long period sampling-frequency ratio detector equipped with the long period counter as unnecessary, or it considers as a high speed and there is no fluctuation of a sampling frequency not much about it, and when fluctuation of a sampling frequency is to some extent large, they are changing the high-speed sampling frequency.

[0075] Furthermore, the sampling-frequency inverter concerning this invention may constitute the sampling-frequency ratio detector 24 of the sampling-frequency inverter of the 2nd example mentioned above, as shown in drawing 10 .

[0076] other examples (henceforth other examples shown in drawing 10) which prepare the sampling-frequency ratio detector shown in this drawing 10 are shown by the above-mentioned (1) formula -- as -- detection value Rn-1 of the past in front of [one twice the value of the present sampling-frequency ratio Rn to] 1 detection period -- subtracting -- a new sampling-frequency ratio -- Rn.NEW is calculated.

[0077] Namely, other examples shown in this drawing 10 supply the sampling-frequency ratio Rn used as the criteria acquired when the sampling-frequency ratio detector 63 carried out counting of the sampling-frequency ratio Fsi of the signal inputted from an input terminal 62 with a dividing clock to an adder circuit 67 through D flip-flop 64 and an inverter circuit 65, and are adding it to the sampling-frequency ratio Rn which minded the bit shift machine 66 in this adder circuit 67. The bit shift machine 66 obtains twice as many value 2Rn as the sampling-frequency ratio Rn, and D flip-flop 64 and an inverter circuit 65 obtain value-Rn-1 of the reverse sign of value Rn-1 in front of 1 detection period of the sampling-frequency ratio Rn. Therefore, in an adder circuit 67, an operation as shown in the above-mentioned (1) formula is performed. Here, the clock counting-down circuit 61 supplies the dividing clock which carried out dividing of the reference clock supplied from an input terminal 60 to the sampling-frequency ratio detector 63 and D flip-flop 64.

[0078] Therefore, other examples shown in this drawing 10 measure the present sampling-frequency ratio Rn from the input sampling frequency Fsi and the output sampling frequency Fso, and are calculating new sampling frequency-ratio Rn.NEW based on detection value Rn-1 of this present detection value Rn and the past. For this reason, a controller 25 can perform stable sampling transform processing, without

not making the buffer memory 13 for re-sampling produce overflow and an underflow, but increasing the capacity of the buffer memory 13 for re-sampling, since the re-sampling time amount address is generable from the value (new sampling-frequency ratio Rn. NEW) which an error like drawing 2 does not accumulate.

[0079] Furthermore, the sampling-frequency inverter concerning this invention may constitute the sampling-frequency ratio detector 24 of the sampling-frequency inverter of the 2nd example mentioned above, as shown in drawing 11 .

[0080] Other examples (henceforth other examples shown in drawing 11) which prepare the sampling-frequency ratio detector shown in this drawing 11 supply the sampling-frequency ratio Rn used as the criteria acquired when the sampling-frequency ratio detector 73 carried out counting of the sampling-frequency ratio Fsi of the signal inputted from an input terminal 72 with a dividing clock to an adder circuit 76 through D flip-flop 74 and an inverter circuit 75, and are adding it to the sampling-frequency ratio Rn in this adder circuit 76. D flip-flop 74 and an inverter circuit 75 obtain value-Rn-1 of the reverse sign of value Rn-1 in front of 1 detection period of the sampling-frequency ratio Rn. therefore, the sampling-frequency ratio Rn current in an adder circuit 76 and the sampling-frequency ratio in front of 1 detection period -- the difference of Rn-1 -- deltaRn is outputted.

[0081] this difference -- deltaRn is supplied to the multiplication circuit 76 and an adder circuit 80. the multiplication circuit 76 -- difference -- the multiplication of the multiplier k (k< 1) is carried out to deltaRn, and the multiplication result kdeltaRn is supplied to an adder circuit 78. an adder circuit 80 -- difference -- accumulation of the output signal of D flip-flop 82 later mentioned to deltaRn is carried out.

[0082] the output signal of an adder circuit 80 is supplied to the multiplication circuit 81 -- having (1-k) -- multiplication is carried out. The output signal of this multiplication circuit 81 is supplied to D flip-flop 82. D flip-flop 82 counting-outputs the value in front of m detection period for the output signal of the above-mentioned multiplication circuit 81 based on the dividing clock supplied from the clock counting-down circuit 71. Therefore, the feedback system circuit which consists of an adder circuit 80, a multiplication circuit 81, and D flip-flop 82 turns into a circuit which asks for the infinite series of m (1-k) (deltaRn-m).

[0083] The infinite series of m (1-k) (deltaRn-m) of this feedback system circuit are added to the multiplication result kdeltaRn from the multiplication circuit 77 in an adder circuit 78. The addition output of this adder circuit 78 is supplied to an adder circuit 79. An adder circuit 79 adds the addition output of an adder circuit 78 to the current sampling-frequency ratio Rn, and outputs new sampling frequency-ratio Rn.NEW.

[0084] Here, the clock counting-down circuit 71 supplies the dividing clock which carried out dividing of the reference clock supplied from an input terminal 70 to the sampling-frequency ratio detector 73, D flip-flop 74, and the D-flip-flop circuit 82.

[0085] Therefore, other examples shown in this drawing 11 kdeltaRn which measured

the current sampling-frequency ratio Rn from the input sampling frequency Fsi and the output sampling frequency Fso, and was obtained from D FURI@PPUFUROPPU 74 and an inverter circuit 75 to this current detection value Rn, the infinite series as a total value of the term to infinity are added from 1 of m of the output (1-k) (deltaRn-m) m of the feedback system circuit which consists of an adder circuit 80, a multiplication circuit 81, and D flip-flop 82, and it is shown in the following (4) types -- as -- a new sampling-frequency ratio -- Rn.NEW has been obtained.

[0086]

[Equation 3]

[0087] Here, it is deltaRn=Rn-Rn -1 and k< 1.

[0088] And other examples shown in this drawing 11 are outputting this new sampling frequency-ratio Rn.NEW to the controller 25. For this reason, a controller 25 can perform stable sampling transform processing, without not making the buffer memory 13 for re-sampling produce overflow and an underflow, but increasing the capacity of the buffer memory 13 for re-sampling, since the re-sampling time amount address is generable from the value (new sampling-frequency ratio Rn. NEW) which an error like drawing 12 does not accumulate.

[0089]

[Effect of the Invention] In the sampling-frequency inverter from which the sampling-frequency inverter concerning this invention changes the sampling frequency of an input signal into the sampling frequency of arbitration A storage means to memorize the above-mentioned input signal, and the interpolation processing means which carries out interpolation processing of the signal read from the above-mentioned storage means, A sampling-frequency ratio detection means to detect the sampling-frequency ratio of the sampling frequency of the above-mentioned input signal, and the sampling frequency of the above-mentioned arbitration, and to detect a new sampling-frequency ratio based on this detection value and the past detection value, Since it has the control means which controls the above-mentioned storage means and the above-mentioned interpolation processing means according to the new sampling-frequency ratio of the above-mentioned sampling-frequency ratio detection means A limit of a change rate and variation is made unnecessary, without not generating accumulation of the error of the re-sampling time-of-day address, and therefore increasing the capacity of buffer memory, even if a sampling-frequency ratio continues changing continuously during 1 scheduled time.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the outline configuration of the sampling-frequency inverter of the 1st example of this invention.

[Drawing 2] It is drawing for explaining actuation of the sampling-frequency ratio detector established in the sampling-frequency inverter of the 1st example shown in drawing 1 .

[Drawing 3] It is the block diagram showing the outline configuration of the sampling-frequency inverter of the 2nd example of this invention.

[Drawing 4] It is the block diagram showing the outline configuration of the sampling-frequency ratio detector of the sampling-frequency inverter of the 2nd example, and a controller shown in drawing 3 .

[Drawing 5] It is drawing for explaining actuation of the interpolation processing circuit of the sampling-frequency inverter of the 2nd example shown in drawing 3 .

[Drawing 6] It is the block diagram showing the outline configuration of the sampling-frequency ratio detector and controller which are used for the sampling-frequency inverter of the 3rd example of this invention.

[Drawing 7] It is drawing for explaining actuation with the short period of the sampling-frequency ratio detector of the sampling-frequency inverter of the 3rd example.

[Drawing 8] It is drawing for explaining actuation with the long period of the sampling-frequency ratio detector of the sampling-frequency inverter of the 3rd example.

[Drawing 9] It is the block diagram showing the outline configuration of the sampling-frequency ratio detector used for the sampling-frequency inverter of other examples of this invention.

[Drawing 10] It is the block diagram showing the outline configuration of the sampling-frequency ratio detector used for the sampling-frequency inverter of other examples in this invention.

[Drawing 11] It is the block diagram showing the outline configuration of the sampling-frequency ratio detector of the sampling-frequency inverter of other examples of this invention.

[Drawing 12] It is drawing for explaining actuation of the sampling-frequency ratio detector of the sampling-frequency inverter of other examples shown in drawing 11 .

[Drawing 13] It is drawing for explaining actuation of the sampling-frequency ratio detector used for the conventional sampling-frequency inverter.

[Description of Notations]

2 Buffer Memory for Re-Sampling

3 Interpolation Processing Circuit

7 Sampling-Frequency Ratio Detector

8 Controller

12 8Fs over Sampling Technique Filter
13 Buffer Memory for Re-Sampling
14 Interpolation Processing Circuit
19 Re-Sampling-Frequency Signal Output Circuit
20 Band Limit Filter